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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,366	09/19/2000	Douglas O. Powell	EN9-99-026	5058

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EXAMINER	
COMPTON, ERIC B	
ART UNIT	PAPER NUMBER
3726	9

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/665,366	POWELL, DOUGLAS O.	
	Examiner	Art Unit	
	Eric B. Compton	3726	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *an RCE filed 5/22/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 22, 2003, has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: removing a layer of conductive material on one of the top and bottom surface, in order to have only one layer remaining on a first surface, to comport with the steps 1-3 of claim 1. The omitted step is clearly shown in Figure 3.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-3, 7-10, 12-14, 16-18, 20-21, 37-42, 45-48, 51- 53, and 64-68, are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,744,758 to Takenouchi et al.

Regarding claims 1, 46, and 68, Takenouchi et al disclose a multi-layered electronic structure and a method for making said structure (see Figures 7(a)-7(e), 8, & 9), comprising the steps of:

a. Providing a plurality of sub-composites (12) comprising: providing a layer of dielectric material (14,16) having a top and bottom;

b. providing a layer of electrically conducting material (13) on one of the top surface of the dielectric layer;

c. forming at least one passage (18) through the dielectric layer;

d. depositing electrically conducting material (32, 34) in at least one of the at least one passage through the dielectric layer;

e. removing portions of the layer of electrically conducting material to define a pattern of circuitry (see Figures 7(d) and 7(e));

f. stacking a plurality of sub-composites (Figure 9);

g. aligning the plurality of sub-composites (it is inherent that the structures are aligned);

h. joining the plurality of sub-composites such that the electrically conducting material in at least one on the at least one the blind vias makes electrically contact by forming a metallurgical bond (see col. 10, lines 65-67) to the conductive pattern (by heat press, col 11, lines 63-65); and

i. filling the spaces between adjacent sub-composites with electrically insulating material (via heat pressing, see Figure 8).

Regarding claims 66 and 67, an electronic package, formed by the method above is shown and described. Furthermore, it is inherent that such structures are used for mounting electrical components.

Regarding claims 2-3, and 47-48, Takenouchi al disclose that the dielectric layer (16) may be polyimide (col 6, line 4)

Regarding claim 7, it is inherent that the conducting material may be solderable (col 9, lines 38-40).

Regarding claims 8-9, 14, and 51-52, Takenouchi et al disclose that the conducting material is copper foil (col 10, line 30).

Regarding claims 10 and 12, Takenouchi et al disclose that the conducting material may be electroplated (col 10, line 38).

Regarding claim 13, this step is inherently accomplished.

Regarding claims 16 and 45, Takenouchi et al disclose that the conducting material is patterned with a resist, which is a protective cover.

Regarding claim 17, Takenouchi et al disclose that the passages may be formed by laser (col 10, line 33).

Regarding claim 18, see Figure 7(e), wherein the conducting material deposited in a passage does not extend beyond the opening of the passage.

Regarding claims 20-21, and 53, Takenouchi et al disclose that the conducting material is a metal deposited in the passages in by platting (col 10, line 5).

Regarding claims 37-41, Takenouchi et al discloses bonding via pressure in a vacuum under inert atmosphere (see col, 10, lines 55-60).

Regarding claims 42, 64, and 65, Takenouchi et al inherently disclose that the structures are filled with a thermoset plastic (16, see col 12, lines 3-5).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-6, 11, 15, 19, 24-33, 35-36, 49-50, 54- 58, and 60-63 are rejected under 35 U.S.C. 103(a) as being unpatentable Takenouchi et al in view of US Patent 4,915,983 to Lake et al.

Takenouchi et al disclose the invention cited above. However, they do not disclose the particulars of the invention as claimed by Applicant.

Lake et al disclose a multi-layered electronic structure and a method for making said structure (see Figure 8) very similar in structure to both Takenouchi et al and Applicant's inventions. Many of the particulars not disclosed by Takenouchi et al are disclosed Lake et al, which are apparently all in the art of forming interconnects.

Regarding claims 4-6, 11, 15, 19, 24-33, 35-36, 49-50, 54- 58, and 60-63, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the sub-composites of Takenouchi et al using the various interconnect forming techniques well-known in the art, in light of the teachings of Lake et al, in order to take advantage of well-known interconnect forming technology, thus saving capital costs on retooling production lines for new product runs.

Regarding claims 4 and 49, Official Notice is taken that liquid crystal polymer film is well known in the circuit board arts and a skilled artisan would have found it obvious at time of invention to use such in the method of Takenouchi et al.

Regarding claims 5, and 50, Lake et al disclose that the dielectric (50) may be polyimide (col 9, line 33) and/or include a mesh or screen of glass (col 10, lines 37-38).

Regarding claim 15, Lake et al disclose that the dielectric material is applied to the foil using a press roll (col 9, line 15).

Regarding claim 6, see Figure 8, step 1 of Lake et al.

Regarding claim 11, Official Notice is taken that applying a coating by physical vapor deposition to a substrate comprising vacuum evaporation or sputtering is well known in the art and a skilled artisan would have found it obvious at time of invention to use such in the method of Takenouchi et al.

Regarding claim 19, see Figure 8, step 5, or Lake et al.

Regarding claims 24-26, 28, 29, 30, 31, 33, 54, 55, and 56, Lake et al disclose a layer of tin lead alloy may be applied over the copper foil by a continuous electroplating process (col 9, lines 57-59).

Regarding claims 27 and 57, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provide a cap having a thickness of 0.0001 to .0004 inch, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 32, Takenouchi et al disclose that the circuitry is formed by resist patterning (col 10, lines 48-50).

Regarding claims 35, 60-62, Official Notice is taken that aligning structure such as providing holes in the laminate layers and a jig having corresponding aligning pins and indicia (registration marks) are well known in the art. Applicant, also alludes to the fact such structures are known, referring to slots and pins as standard alignment means (page 34, lines 2-3).

Regarding Claims 36 and 63, Lake et al disclose that the layers will be soldered coated (col 9, line 39).

Regarding claim 58, Official Notice is taken that coating a substrate with oxides (e.g. tin oxide) are known in the art to roughen the surface for subsequent bonding and a skilled artisan would have found it obvious at time of invention to apply a coating for such purpose.

8. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al in view of US Patent 3,601,523 to Arndt.

Takenouchi et al disclose the invention cited above. However, they do not disclose that the conducting material provided in the passage is a conducting paste.

Arndt discloses a method for filling a passageway with a conducting paste in order to conductively contact the circuitry from one side of a dielectric to another.

Regarding claim 22, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a conducting paste in the passage of Takenouchi et al, in light of the teachings of Arndt, in order to provide a more low resistant connection than by platting (see col 1, lines 60+).

Regarding claim 23, Arndt uses a squeegee (20) to apply the conducting paste.

9. Claims 34 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al in view of US Patent 4,921,157 to Dishon et al.

Takenouchi et al disclose the invention cited above. However, they do not disclose treating the dielectric layer and patterned circuitry with fluorine-containing plasma.

Dishon et al disclose a method for treating a circuit board with exposed soldering. The surfaces are treated with a fluorine-containing plasma in order to remove oxides and provide a more efficient solder joint.

Regarding claims 34 and 59, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have treated the structure of

Takenouchi et al with fluorine-containing plasma, in light of the teachings of Dishon et al, in order to remove surface oxides from the solder contacts.

10. Claims 37-44 and 69-78 rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al in view of US Patent 5,635,010 to Pepe et al.

Takenouchi et al disclose the invention cited above. The reference relies on pressure and heat to bond the structures. However, it does not specifically disclose providing filling the spacing between adjacent structures with a liquid, which is transformed into a solid.

Pepe et al disclose a method for bonding layers to form a laminate (see Figures 9-12). A dielectric adhesive, preferably a polyimide, applied as a liquid is provide on the to close voids and help bond substrates together. "The preferred polyimide exhibits sufficient viscous flow at the initial temperature and pressure conditions such that it fills all voids between adjacent chips and excess adhesive extrudes from the chip stack to achieve minimal thickness of the adhesive layer" (col 7, lines 58-63).

Regarding claims 37 and 69, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided a liquid insulator to bond the structures of Takenouchi et al, in light of the teachings of Pepe et al, in order to fill the voids between the structures.

Regarding claims 37-44, and 76-78, see col 8, lines 49-64 of Pepe et al regarding bonding with pressure in a vacuum with an inert atmosphere.

Regarding claims 70-71, the liquid may include epoxy, an organic resin.

Regarding claims 73-74, Official Notice is taken that inorganic filler and cross-linking is the art to provide structures of added strength and that a skilled artisan would have found it obvious at the time of invention to have provided either for such purpose.

Regarding claim 74, it is inherent that the liquid resin is moved by capillary action.

Regarding claim 75, the liquid resin is placed on the top periphery of the structures.

Response to Arguments

11. Applicant's arguments filed May 22, 2003, have been considered but they are not found fully persuasive.

Applicant's arguments with respect to the claim objections are persuasive. Therefore, these objections have been withdrawn.

Applicant did not address the 112, second rejection with respect to claim 6.

Applicant argues that the prior art, mainly Takenouchi et al, does not disclose "processing the paste so as to form metallurgical bonds." Paper No. 6, pg. 6. Applicant's amendment to the claims recites,

> joining said plurality of sub-composites such that the electrically conducting paste material in at least one of said blind vias makes electrical contact by forming a metallurgical bond to the conductive pattern on an adjacent sub-composite;

Support for this amendment is indicated by Applicant to be on page 8, lines 13-16 and page 27, lines 2-16 of the specification. Applicant relies on a conductive paste having conductive particles dispersed in an organic resin. *See* Specification, page 27.

Takenouchi et al rely on an identical type of paste, comprising conductive particles disposed in a thermoplastic resin. *See* col. 9, lines 48-57. Applicant further discloses that during the joining of the sub-composites, at around or less than 300°C, causes curing of the conductive paste causing a metallurgical bond between the conductive paste particles and/or metal surfaces in contact with the paste. *See* Specification, page 27. Takenouchi et al disclose that the sub-components are joined between a range of 220 and 300 °C. *See* col. 10, lines 55-60. Furthermore, Takenouchi et al disclose that, "Since the electro-conductive thermoplastic resin layer 34 is also softened to be adhesive during the heat pressing, the via 30 and the circuit pattern 22 are tightly bonded together." *See* col. 10, lines 65-67. Thus, the method of Takenouchi et al, will accomplish the metallurgical bonding (as claimed), in as much as Applicant's invention contemplates.

Applicant's arguments with respect to the obviousness rejection are essentially moot.

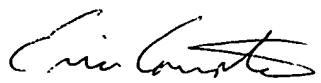
Therefore, the rejections above are valid.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Compton whose telephone number is (703) 305-0240. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory M. Vidovich can be reached on (703) 308-1513. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9302 for regular communications and (703) 872-9303 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1148.



Eric Compton
Patent Examiner
A/U 3726

June 13, 2003